23.8 A 75-GHz PLL in 90-nm CMOS Technology

Jri Lee

National Taiwan University, Taipei, Taiwan

Phase-locked loops (PLLs) continue to play critical roles in ultra high-speed communication systems. The design and experimental verification of a 75GHz PLL, fabricated in a 90nm CMOS technology, are presented in this paper. Figure 23.8.1 shows the PLL architecture. The fully integrated PLL consists of a differential VCO, a divider chain with total modulus of 64, a phase and frequency detector (PFD), and a third-order loop filter. The VCO incorporates short-circuited $3\lambda/4$ lines to achieve high oscillation frequency and low phase noise. Different divider topologies, injection locked [1], Miller [2], and static, are used and placed in descendant order of frequency to accommodate the severe tradeoffs between the input frequency and operation range. Careful loading adjustments and EM simulations are conducted to ensure robust locking between the VCO and dividers. Based on single-sideband (SSB) mixers, the proposed PFD obviates traditional pulse-width comparison, and suppresses the reference feedthrough significantly. Similar to [3], the phase locking and frequency acquisition loops are decomposed, and the frequency detector along with its V/I converter are automatically turned off upon lock to minimize the disturbance to the VCO.

Figure 23.8.2 depicts the VCO and the first divider stage. Transmission lines equivalent to $3\lambda/4$ of a 75GHz clock are used to distribute the capacitive loading and boost the oscillation frequency. Having one end short-circuited and the other end open-circuited, these lines resonate differentially with the cross-coupled pair M_1-M_2 providing negative resistance. Connecting to the 1/3 points of the lines (nodes A and A'), this pair forces the transmission lines to create peak swings at these nodes. The waves propagate and reflect along the lines and form the second maximum swings with opposite polarities at nodes B and B'. That is, node A (A') and node B (B') are 180° out of phase. As a result, the buffers (M_3-M_4), dividers (M_5-M_6), and varactors (M_7-M_8) can be moved to these ends, making the two zenith positions bear approximately equal capacitance. This arrangement reduces the effective loading and raises the oscillation frequency. To achieve high Q and compact layout, the transmission lines are actually realized as three identical inductors in series. Two layers of ground shields made of ploysilicon and metal1 are placed alternately underneath the spirals. The natural biasing established by M_1-M_2 pair facilitates DC coupling between the VCO and subsequent blocks. Careful layout arrives at perfect symmetry between the loadings at nodes B and B'. Inductor L_R is added to resonate out the parasitic capacitance associated with nodes C and C', allowing stronger signal injection through M_5 and M_6.

The VCO is biased with a supply-independent circuit M_9-M_{12} and R_S. To further reject the supply noise, M_{13} is used to absorb extra current variation caused by channel-length modulation. That is, to set $|\partial I_{SS}/\partial V_{DD}| = |\partial I_C/\partial V_{DD}|$ and let the current flowing into M_1-M_2 pair (I_{TANK}) remain constant. It leads to a fixed voltage at node P, leaving the resonance frequency insensitive to supply perturbation. The power penalty of M_{13} can be restrained to as low as 20% with proper design.

To avoid generating on-off pulses which potentially create reference spurs, phase detection is performed by mixing two quadrature signals, one from the reference input (CK_{ref}, provided by a static divided-by-2 circuit) and the other from the last divider stage (CK_{div}). As shown in Fig. 23.8.3, the phase detector distills the phase error and reveals a sinusoidal characteristic. The V/I converter thus pumps a proportional current, either positive or negative, into the loop filter and changes the control voltage accordingly. Since the characteristic can be approximately considered linear in the vicinity of origin and no pulse generation is involved, it achieves a truly quiet phase examination and reference spurs are significantly reduced. Note that current imbalance in the V/I converter can no longer be an issue in this design. In the presence of mismatches, finite "image" will be observed at $2\omega_{in}$. A low-pass filter with corner frequency of 8.3MHz is placed right after the SSB mixer to suppress the image by more than 40dB.

The periodic characteristic of the phase detector implies a limited capture range. Fortunately, the frequency error can be discerned by introducing another SSB mixer. As illustrated in Fig. 23.8.4, the two outputs V_{PD} and V_2 appear with 90° phase difference. Whether the former is leading or lagging the latter depends on the sign of $\Delta\omega_{in}$, which can be easily obtained by using a flip-flop to sample one signal with the other. Note that the very slow sinusoids of V_{PD} and V_2 would cause malfunction of the flip-flop, since the fluctuations due to coupling and noise make the transitions ambiguous. To remedy this issue, two hysteresis buffers are used to sharpen the waveforms with clear transitions. The automatic switching-off function is accomplished by applying *ENFD* to $(V/I)_{FD}$ and making it disabled when the loop is locked.

The PLL is fabricated in a 90nm CMOS technology and tested on a high-speed probe station. The circuit achieves an operation range of 320MHz. It functions properly with any supply voltage between 1.35V and 1.55V. The total power consumption with from a 1.45V supply (excluding I/O buffers) is 88mW, of which 8mW is dissipated in the VCO, 66mW in the divider chain, and 14mW in the PFD and V/I converters. The reference input level can be as low as –16dBm.

Figure 23.8.5 depicts the output spectra of the VCO and the first divider under locked condition. The phase noise at 100kHz offset measures –88 and –94dBc/Hz, respectively. At these high frequencies, the spectrum analyzer must incorporate harmonic mixers which introduce 40 to 50dB loss, resulting in a limited range on sideband measurement. It is observed that the reference spurs are buried in the noise floor, which is 72dB lower than the carrier. Thus, it is concluded that the reference sidebands are less than –72dBc.

Figure 23.8.6 plots the 75GHz output waveform, where the peak-to-peak and rms jitter measures 609 and 87fs, respectively. The 37.5GHz output presents jitter of $2.15ps_{pp}$ and $293fs_{rms}$. The inductor Q of the VCO is estimated to be 16 at 75GHz, and the loop bandwidth is equal to 2.5MHz. Figure 23.8.7 shows the die micrograph which occupies $1.0\times0.8mm^2$ including pads.

Acknowledgments:
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References:
[1] H.R. Rategh and T.H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE J. Solid-State Circuits*, vol. 34, pp. 813-821, June, 1999.
[2] Jri Lee and Behzad Razavi, "A 40-GHz Frequency Divider in 0.18μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 39, pp. 594-601, April, 2004.
[3] Jri Lee, "High-Speed Circuit Designs for Transmitters in Broadband Data Links," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1004-1015, May, 2006.

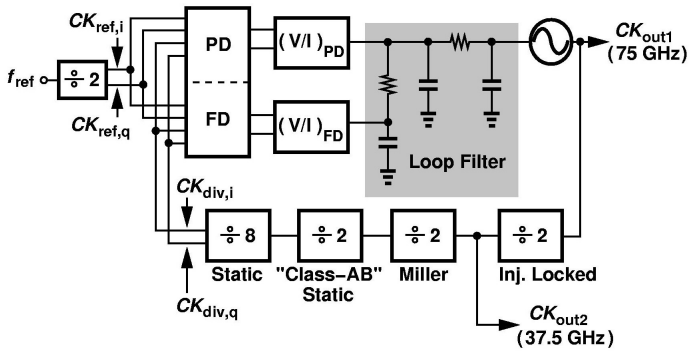

Figure 23.8.1: PLL architecture.

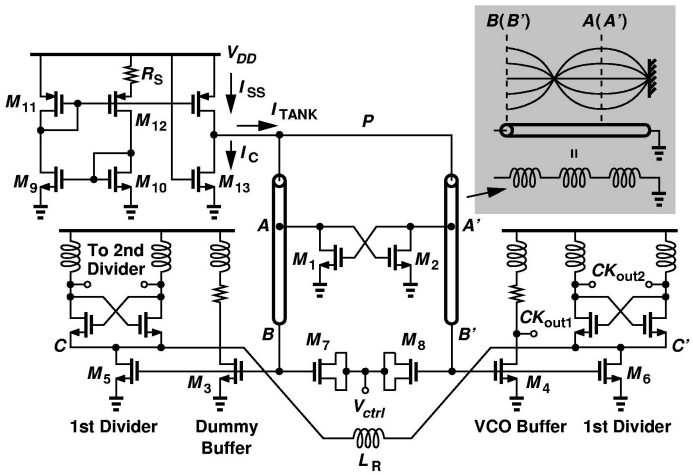

Figure 23.8.2: VCO and first divider.

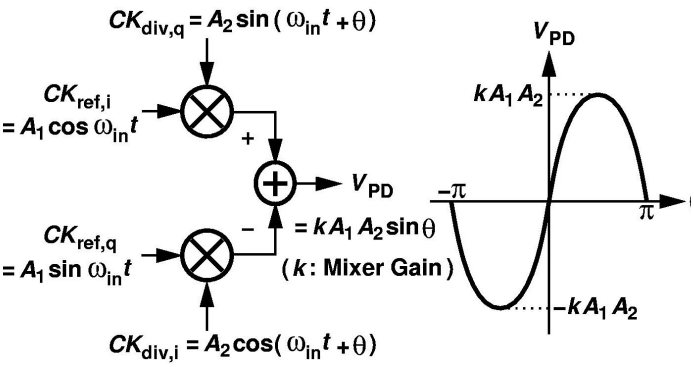

Figure 23.8.3: Operation of phase detector.

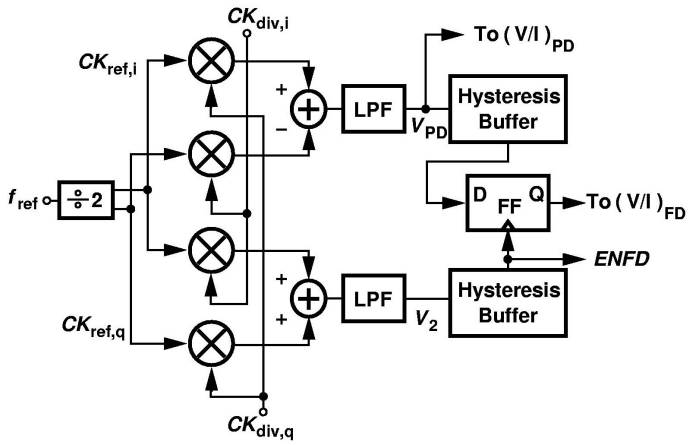

Figure 23.8.4: Complete phase and frequency detector.

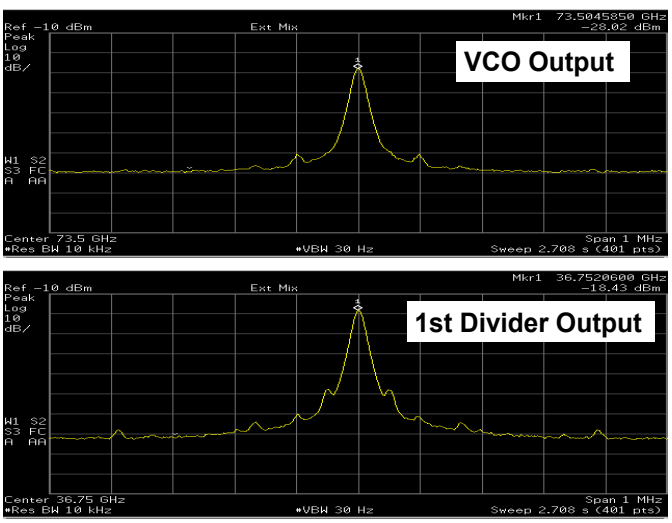

Figure 23.8.5: Output spectra of VCO and first divider.

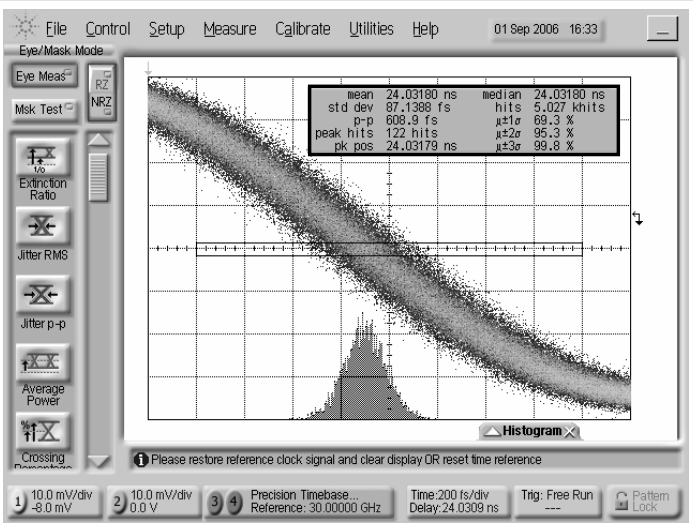

Figure 23.8.6: Measured waveforms of the 75GHz output (horizontal scale: 200fs/div, vertical scale: 10mV/div).

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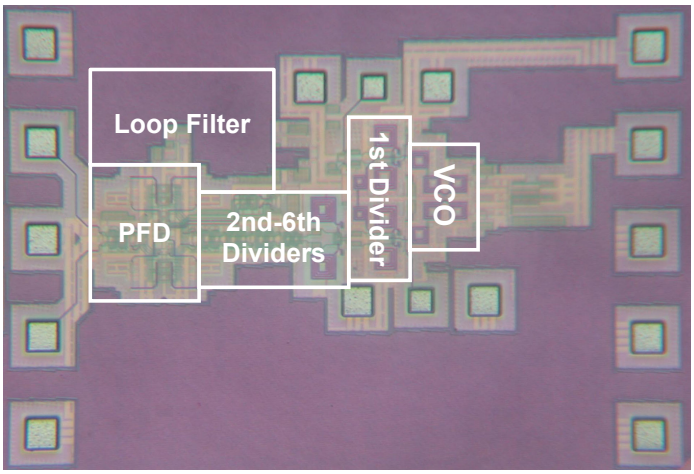

Figure 23.8.7: Chip micrograph.

